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MiniCirc v1.1

The Cadence AIG SAT-solver MiniCirc v1.1 consists of an in-house implementation of the ideas presented in [2] for combining logic synthesis and SAT solving. MiniCirc starts by minimizing the And-Inverter-graph by *DAG-aware rewriting*, then translates the resulting graph to CNF by *technology mapping for CNF*; restricted to 4-input cuts for efficiency reasons. Finally, an improved version of MiniSat 2.0 [4, 3, 1] is run, which includes CNF-preprocessing.

About the submission

The authors of this submission are: Niklas Een (Cadence Research Laboratories) and Niklas Sörensson (Chalmers University of Technology). The solver was written in C++ and compiled for 64-bit Linux. The modifications to MiniSat 2.0 are documented in the description of this year's MiniSat submission for the main CNF competition.

References

[1] Niklas Een and Armin Biere. **Effective Preprocessing in SAT through Variable and Clause Elimination**. In *Proc. of Theory and Applications of Satisfiability Testing, 8^{th} International Conference (SAT'2005)*, volume 3569 of *LNCS*, 2005.

[2] Niklas Een, Alan Mishchenko, and Niklas Sörensson. **Applying Logic Synthesis for Speeding Up SAT**. In *Proc. of Theory and Applications of Satisfiability Testing, 10^{th} International Conference (SAT'2007)*, volume 4501 of *LNCS*, 2007.

[3] Niklas Een and Niklas Sörensson. **MiniSat – A SAT Solver with Conflict-Clause Minimization**. http://www.cs.chalmers.se/Cs/-Research/FormalMethods/MiniSat/cgi/MiniSat_v1.13_short.ps.gz.cgi.

[4] Niklas Een and Niklas Sörensson. **An Extensible SAT Solver**. In *Proc. of Theory and Applications of Satisfiability Testing, 6^{th} International Conference (SAT'2003)*, volume 2919 of *LNCS*, 2003.